



TFT LCD Approval Specification

MODEL NO.: N154I3-L02

Customer : Dell

Approved by : _____

Note :

記錄	工作	審核	角色	投票
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- CONTENTS -

REVISION HISTORY	-----	3
1. GENERAL DESCRIPTION	-----	4
1.1 OVERVIEW		
1.2 FEATURES		
1.3 APPLICATION		
1.4 GENERAL SPECIFICATIONS		
1.5 MECHANICAL SPECIFICATIONS		
2. ABSOLUTE MAXIMUM RATINGS	-----	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT		
2.2 ELECTRICAL ABSOLUTE RATINGS		
2.2.1 TFT LCD MODULE		
2.2.2 BACKLIGHT UNIT		
3. ELECTRICAL CHARACTERISTICS	-----	7
3.1 TFT LCD MODULE		
3.2 BACKLIGHT UNIT		
4. BLOCK DIAGRAM	-----	11
4.1 TFT LCD MODULE		
4.2 BACKLIGHT UNIT		
5. INPUT TERMINAL PIN ASSIGNMENT	-----	12
5.1 TFT LCD MODULE		
5.2 BACKLIGHT UNIT		
5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL		
5.4 COLOR DATA INPUT ASSIGNMENT		
5.5 EDID DATA STRUCTURE		
5.6 EDID SIGNAL SPECIFICATION		
6. INTERFACE TIMING	-----	18
6.1 INPUT SIGNAL TIMING SPECIFICATIONS		
6.2 POWER ON/OFF SEQUENCE		
7. OPTICAL CHARACTERISTICS	-----	20
7.1 TEST CONDITIONS		
7.2 OPTICAL SPECIFICATIONS		
8. PRECAUTIONS	-----	24
8.1 HANDLING PRECAUTIONS		
8.2 STORAGE PRECAUTIONS		
8.3 OPERATION PRECAUTIONS		
9. PACKING	-----	25
9.1 CARTON		
9.2 PALLET		
10. DEFINITION OF LABELS	-----	27
10.1 CMO MODULE LABEL		
10.2 CARTON LABEL		

**CHI MEI**
OPTOELECTRONICS CORP.Doc No.:
Issued Date: Nov, 13, 2008
Model No.: N154I3-L02**Approval****REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 3.0	Nov,13, 2008	All	All	Approval specification first issued.



1. GENERAL DESCRIPTION

1.1 OVERVIEW

N154I3-L02 is a 15.4" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1280 x 800 Wide-XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- WXGA (1280 x 800 pixels) resolution
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	331.2 (H) x 207.0 (V) (15.4" diagonal)	mm	(1)
Bezel Opening Area	334.7 (H) x 210.5 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.2588 (H) x 0.2588 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-glare	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	343.5	344.0	344.5	mm	Module Size
	Vertical(V)	221.5	222.0	222.5	mm	
	Thickness(T)	-	6.0	6.2	mm	
Glass Thickness	TFT	0.45	0.5	0.55	Mm	Glass Thickness
	CF	0.45	0.5	0.55	Mm	
Weight		-	510	525	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

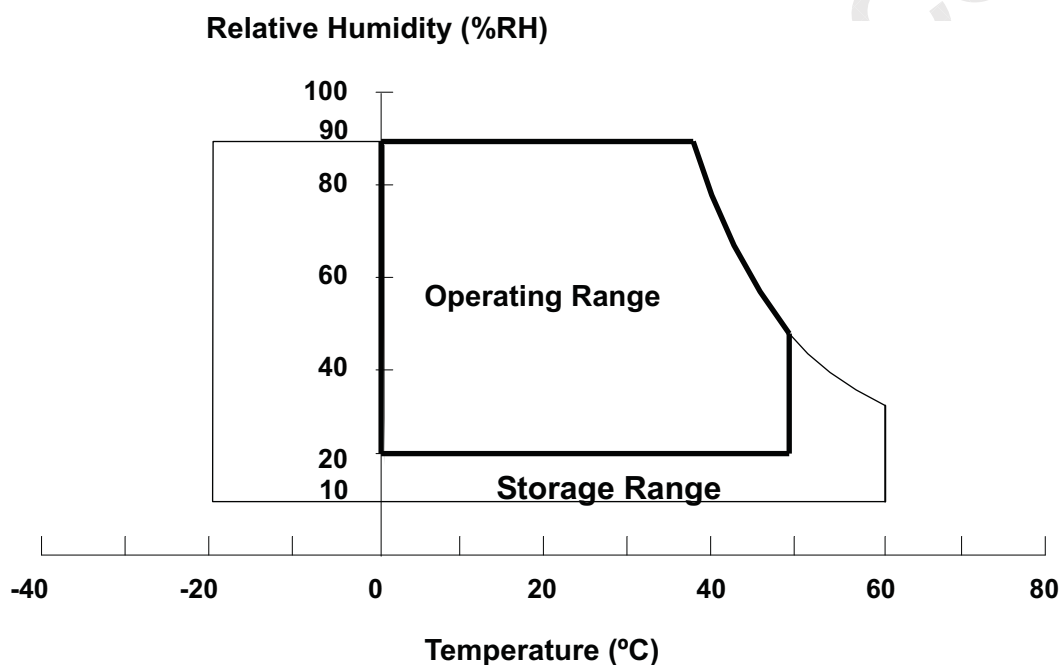
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface area should be 0 °C min. and 60 °C max.

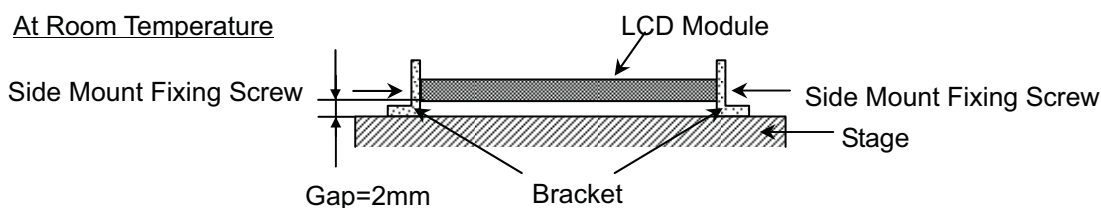


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~500 Hz, 30 min/cycle, 1cycle for X,Y,Z-axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CC} +0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _L	-	2.5K	V _{RMS}	(1), (2), I _L = 6.0 mA
Lamp Current	I _L	2.0	7.0	mA _{RMS}	
Lamp Frequency	F _L	50	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

 $T_a = 25 \pm 2^\circ\text{C}$

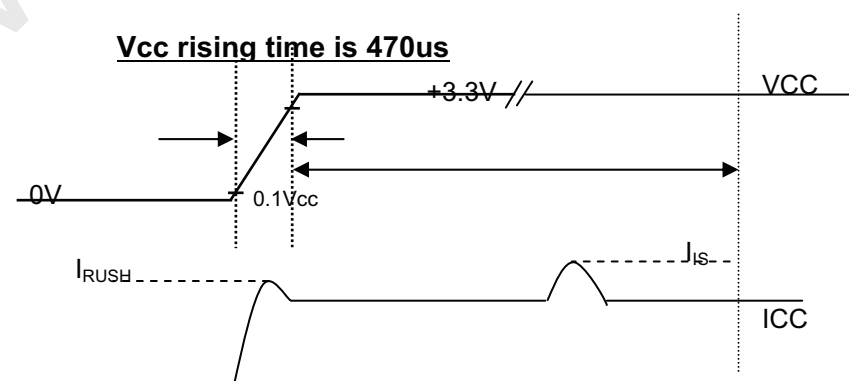
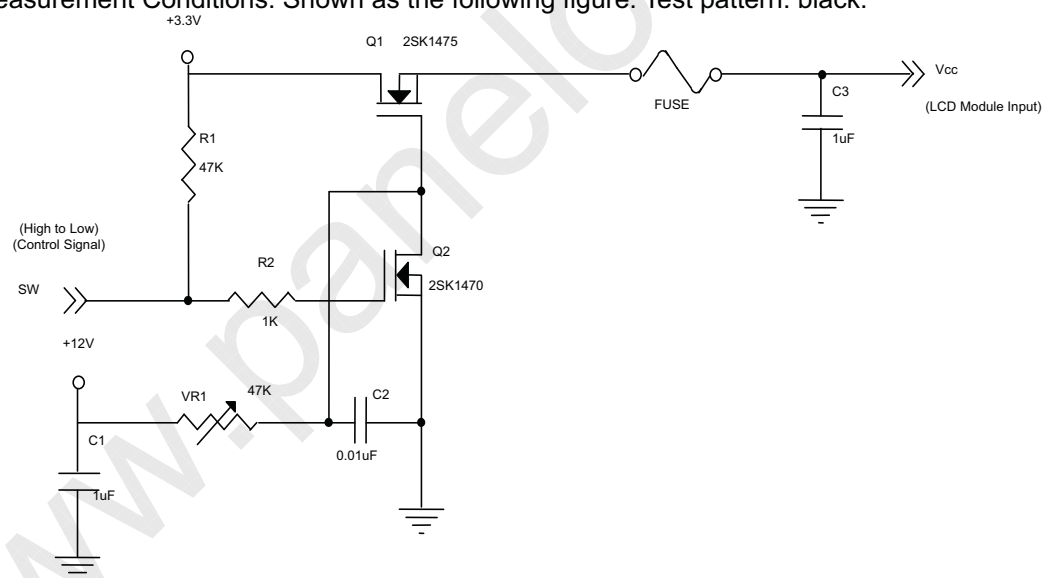
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	50		mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	I_{CC}	-	320	-	mA	(3)a
	Black		-	380	480	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), $V_{CM}=1.2V$
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5) $V_{CM}=1.2V$
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$ V_{ID} $	100	-	600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	3.86	-	W	(4)

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

Note (2) I_{RUSH} : the maximum current when V_{CC} is rising

I_{IS} : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



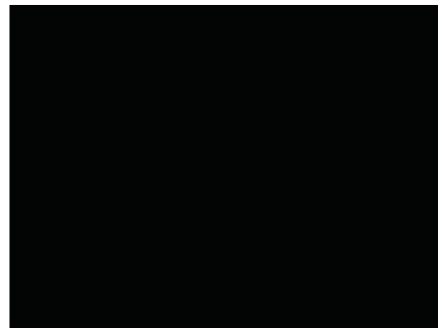
Note (3) The specified power supply current is under the conditions at $V_{CC} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern



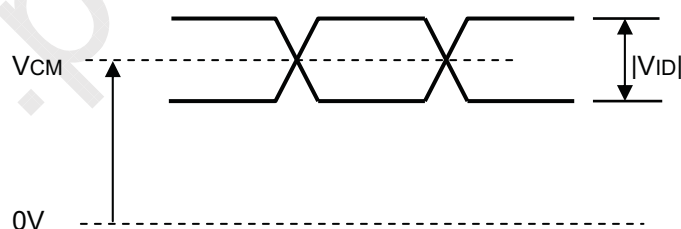
Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

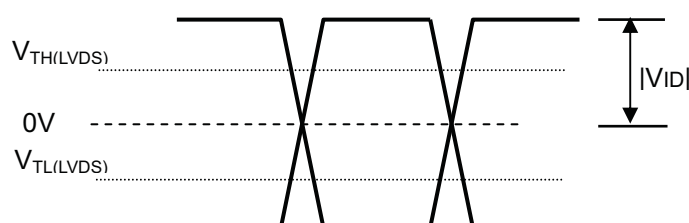
- (a) $V_{CC} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from Sumida.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential

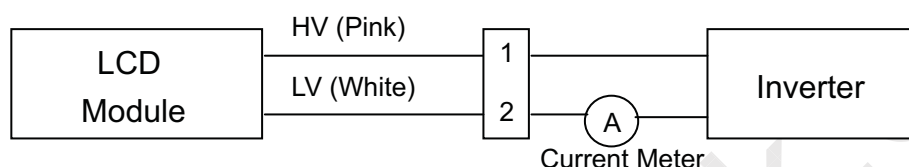


3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Backlight Structure		Conventional B/L				
Lamp Input Voltage	V _L	675	730	945	V _{RMS}	I _L = 6.0 mA
Lamp Current	I _L	2.0	6.0	7.0	mA _{RMS}	(1),(2)
		3.0				(1),(3)
Lamp Turn On Voltage	V _S	-	-	1140(25 °C)	V _{RMS}	(4)
		-	-	1580(0 °C)	V _{RMS}	(4)
Operating Frequency	F _L	50	-	80	KHz	(5)
Lamp Life Time	L _{BL}	15,000	-	-	Hrs	(7)
Power Consumption	P _i	-	4.38	-	W	(6). I _L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) for burst mode inverter design

Note (3) for continuous mode inverter design

Note (4) The voltage that must be larger than V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (5) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (6) $P_L = I_L \times V_L$

Note (7) The lifetime of lamp is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$ and $I_L = 6.0 \text{ mA}_{RMS}$ until one of the following events occurs:

(a) When the brightness becomes $\leq 50\%$ of its original value.

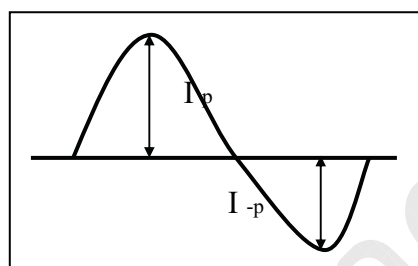
(b) When the effective ignition length becomes $\leq 80\%$ of its original value. (The effective ignition length is a scope that luminance is over 70% of that at the center point.)

Note (8) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below;
- The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
- The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

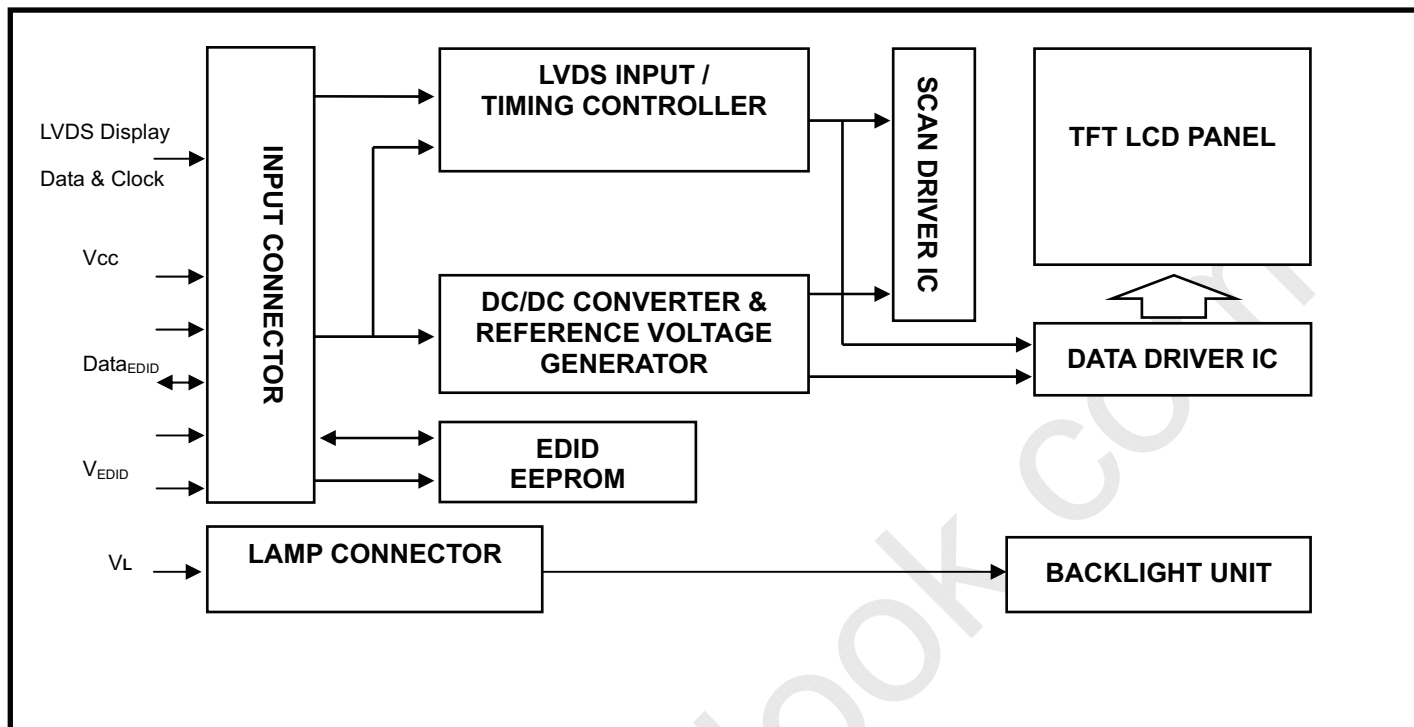
$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

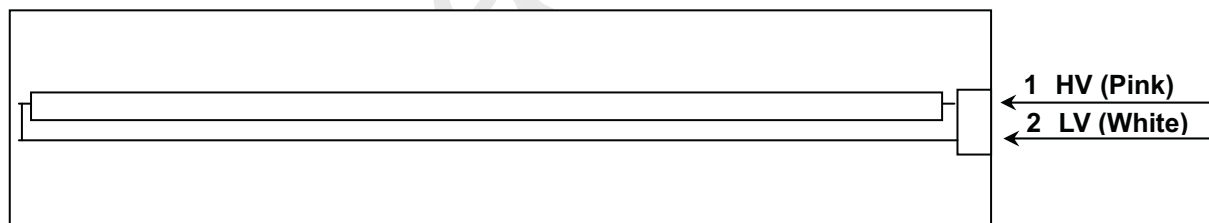
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

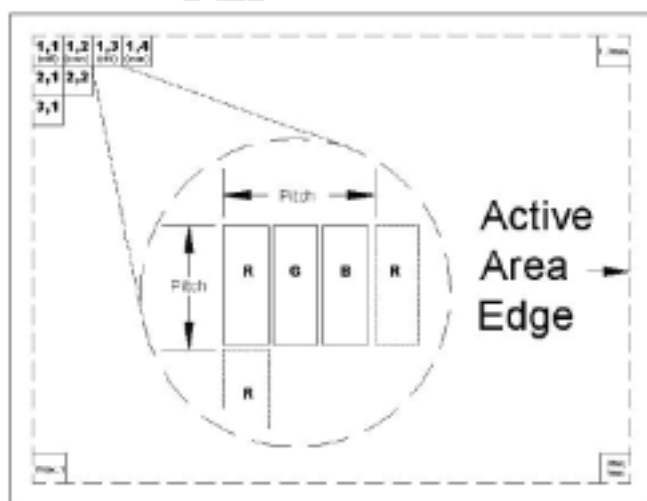
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	NC	Non-Connection		
6	CLK _{EDID}	DDC Clock		DDC Clock
7	DATA _{EDID}	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5, G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5, DE, Hsync, Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	Vss	Ground		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	Vss	Ground		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	Vss	Ground		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) Connector Part No.: JAE FI-XB30SL-HF10 or equivalent

Note (2) User's connector Part No: FI-X30M or equivalent

Note (3) The first pixel is odd as shown in the following figure.



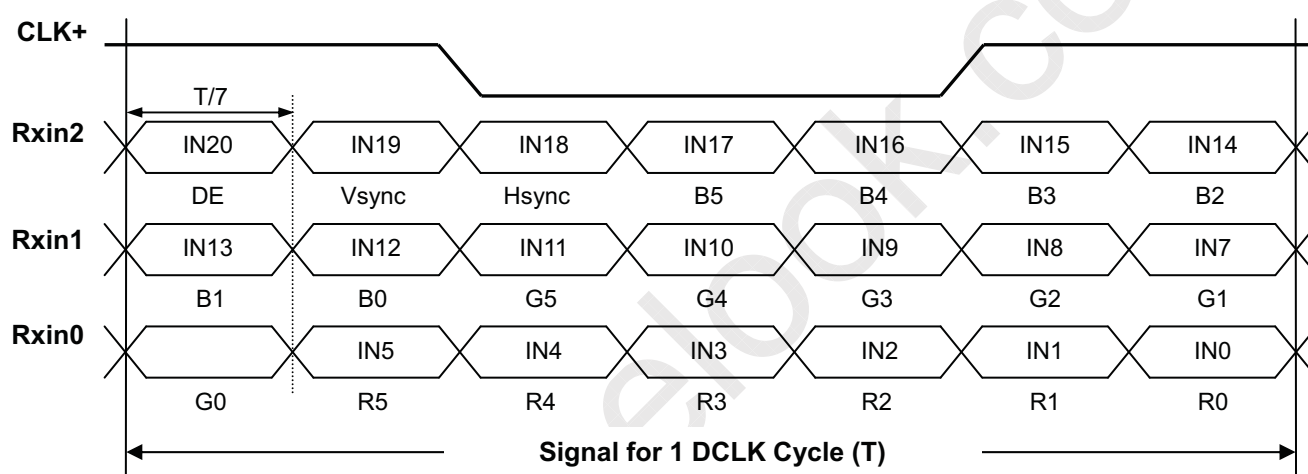
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL





5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage



5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD/ standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N154I3-L02)	38	00111000
11	0B	ID product code (hex LSB first; N154I3-L02)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed "00H")	0C	00001100
17	11	Year of manufacture (fixed "00H")	11	00010001
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	90	10010000
21	15	Active area horizontal 33cm	21	00100001
22	16	Active area vertical 21cm	15	00010101
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	87	10000111
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	F5	11110101
27	1B	Rx=0.58	94	10010100
28	1C	Ry=0.34	57	01010111
29	1D	Gx=0.31	4F	01001111
30	1E	Gy=0.55	8C	10001100
31	1F	Bx=0.155	27	00100111
32	20	By=0.155	27	00100111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1280*800@60Hz)	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001



Doc No.:
Issued Date: Nov, 13, 2008
Model No.: N154I3-L02

Approval

40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("71MHz", According to VESA CVT Rev1.1)	BC	10111100
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active ("1280")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1280 : 160")	50	01010000
59	3B	# 1 V active ("800")	20	00100000
60	3C	# 1 V blank ("23")	17	00010111
61	3D	# 1 V active : V blank ("800 :23")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("331 mm")	4B	01001011
67	43	# 1 V image size ("207 mm")	CF	11001111
68	44	# 1 H image size : V image size ("331 : 207")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
72	48	Detailed timing description # 2 Pixel clock ("71MHz", According to VESA CVT Rev1.1)	BC	10111100
73	49	# 1 Pixel clock (hex LSB first)	1B	00011011
74	4A	# 1 H active ("1280")	00	00000000
75	4B	# 1 H blank ("160")	A0	10100000
76	4C	# 1 H active : H blank ("1280 : 160")	50	01010000
77	4D	# 1 V active ("800")	20	00100000
78	4E	# 1 V blank ("23")	17	00010111
79	4F	# 1 V active : V blank ("800 :23")	30	00110000
80	50	# 1 H sync offset ("48")	30	00110000
81	51	# 1 H sync pulse width ("32")	20	00100000
82	52	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
83	53	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000



Doc No.:
Issued Date: Nov, 13, 2008
Model No.: N154I3-L02

Approval

84	54	# 1 H image size ("331 mm")	4B	01001011
85	55	# 1 V image size ("207 mm")	CF	11001111
86	56	# 1 H image size : V image size ("331 : 207")	10	00010000
87	57	# 1 H boarder ("0")	00	00000000
88	58	# 1 V boarder ("0")	00	00000000
89	59	# 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Model Name "N154I3", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# Dell P/N " FR037" 1st character ("F")	46	01000110
96	60	# Dell P/N " FR037" 1st character ("R")	52	01010010
97	61	# Dell P/N " FR037" 1st character ("0")	30	00110000
98	62	# Dell P/N " FR037" 1st character ("3")	33	00110011
99	63	# Dell P/N " FR037" 1st character ("7")	37	00110111
100	64	LCD Supplier EEDID Revision #: "0"	80	10000000
101	65	Manufacturer P/N ("N")	4E	01001110
102	66	Manufacturer P/N ("1")	31	00110001
103	67	Manufacturer P/N ("5")	35	00110101
104	68	Manufacturer P/N ("4")	34	00110100
105	69	Manufacturer P/N ("I")	49	01001001
106	6A	Manufacturer P/N ("3")	33	00110011
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	00	00000000
112	70	Flag	00	00000000
113	71	SMBUS value @ 10nits = 0d	00	00000000
114	72	SMBUS value @ 17nits = 0d	00	00000000
115	73	SMBUS value @ 24nits = 0d	00	00000000
116	74	SMBUS value @ 30nits = 0d	00	00000000
117	75	SMBUS value @ 60nits = 0d	00	00000000
118	76	SMBUS value @ 100nits = 0d	00	00000000
119	77	SMBUS value @ 180nits = 0d	00	00000000
120	78	SMBUS value @ max nits = 0d	00	00000000
121	79	Bit[1:0] 00:reserved , 01: single LVDS, 10: dual LVDS, 11: reserved Bit[2] 0: No RTC support , 1: RTC support, Bit[7:3] Reserved	01	00000001
122	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	F7	11110111

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

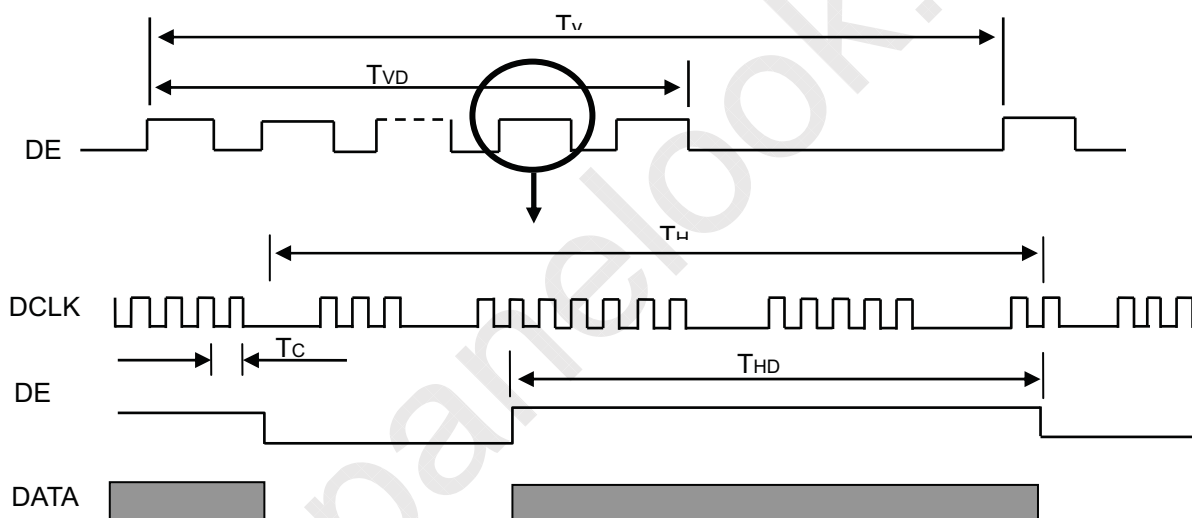
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	66	71	73	MHz	(2)
DE	Vertical Total Time	TV	802	823	840	TH	-
	Vertical Active Display Period	TVD	800	800	800	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	23	TV-TVD	TH	
	Horizontal Total Time	TH	1380	1440	1450	Tc	(2)
	Horizontal Active Display Period	THD	1280	1280	1280	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	(2)

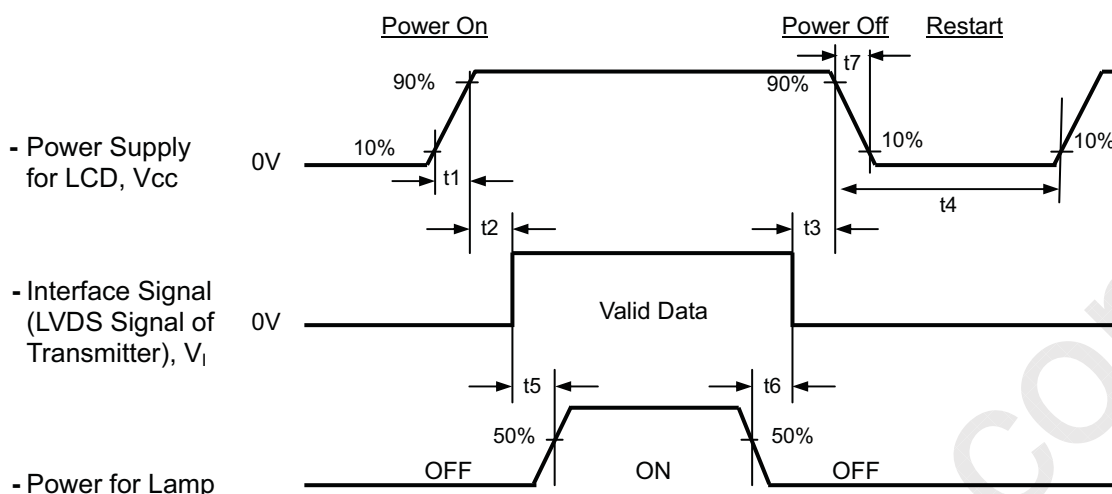
Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 1 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

- $0.5 < t_1 \leq 10 \text{ msec}$
- $0 < t_2 \leq 50 \text{ msec}$
- $0 < t_3 \leq 50 \text{ msec}$
- $t_4 \geq 500 \text{ msec}$
- $t_5 \geq 200 \text{ msec}$
- $t_6 \geq 200 \text{ msec}$

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD V_{cc} to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the V_{cc} falling time is better to follow $5\text{ms} \leq t_7 \leq 300 \text{ ms}$.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

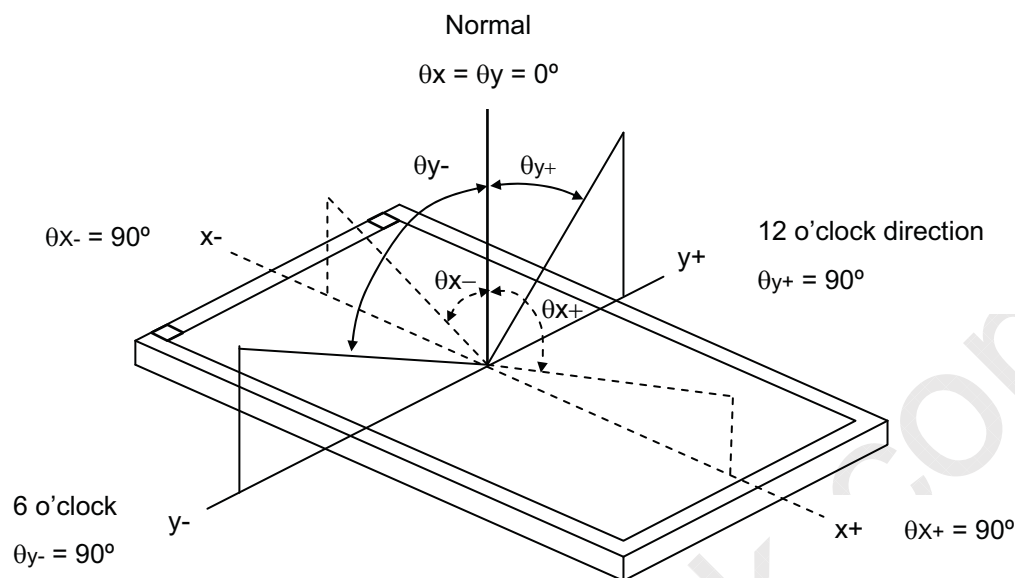
Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	6.0	mA
Inverter Driving Frequency	F _L	61	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	400	500	-	-	(2), (5)
Response Time		T _R		-	3	8	ms	(3)
		T _F		-	5	12	ms	
Average Luminance of White		L _{AVE}		200	220	-	cd/m ²	(4), (5)
Color Chromaticity	Red	R _x		TYP. -0.02	TYP. +0.02	-	(1)	
		R _y				-		
	Green	G _x				-		
		G _y				-		
	Blue	B _x				-		
		B _y				-		
	White	W _x				-		
		W _y				-		
Viewing Angle	Horizontal	θ _x +	CR≥10	40	45	-	Deg.	(1),(5)
		θ _x -		40	45	-		
	Vertical	θ _y +		15	20	-		
		θ _y -		40	45	-		
White Variation of 5 Points		δW _{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	80	-	-	%	(5),(6)

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

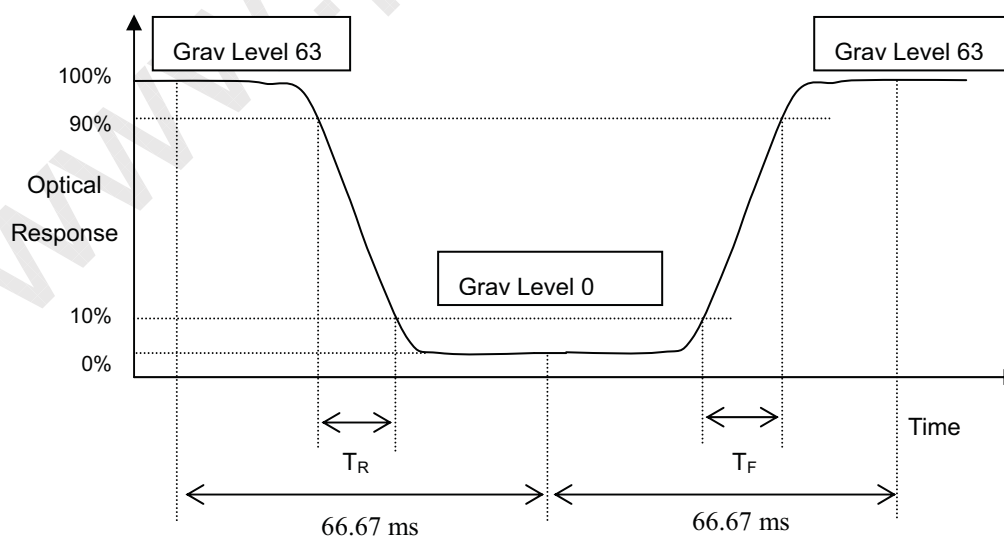
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

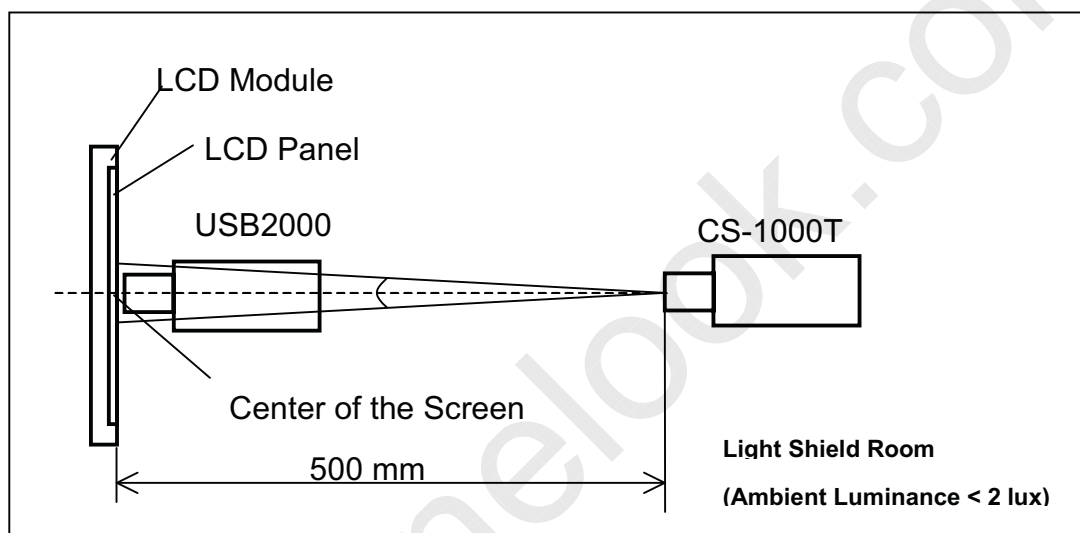
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

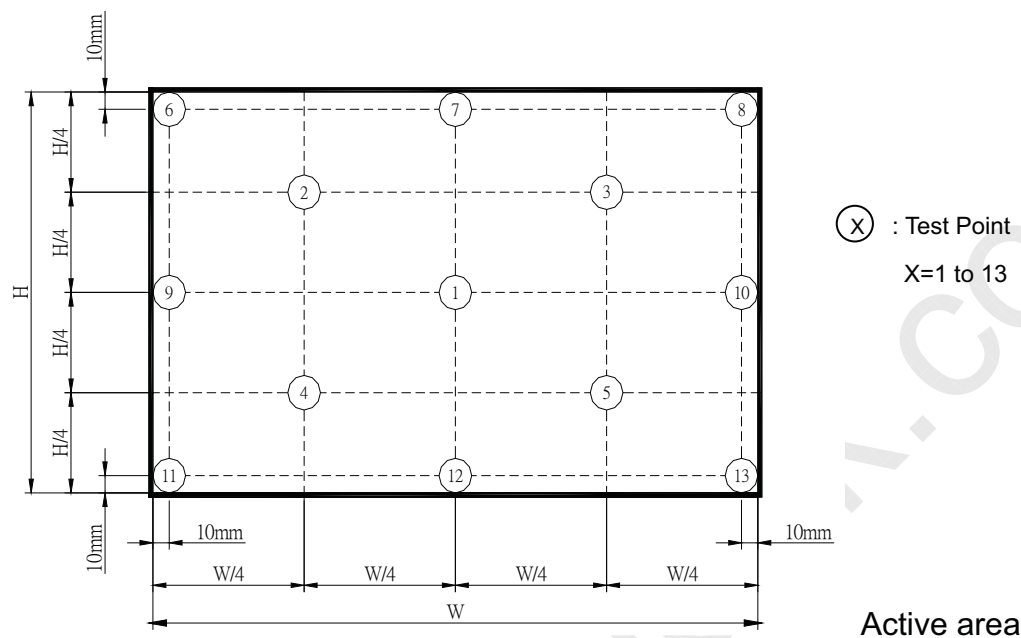
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \text{Minimum} [L(1) + L(2) + L(3) + L(4) + L(5)] / \text{Maximum} [L(1) + L(2) + L(3) + L(4) + L(5)]$$



8. PRECAUTIONS

8.1 SYSTEM MATCHING PRECAUTIONS

- (1) Refer to the drawing.
- (2) To avoid wireless noise interference, please keep the antenna away from LCD control board.

8.2 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.3 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.



Doc No.:
Issued Date: Nov, 13, 2008
Model No.: N154I3-L02

Approval

8.4 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9. PACKING

9.1 CARTON

Box Dimensions : 435(L)*350(W)*325(H)
Weight: Approx. 13.28kg(20 module .per. 1 box)

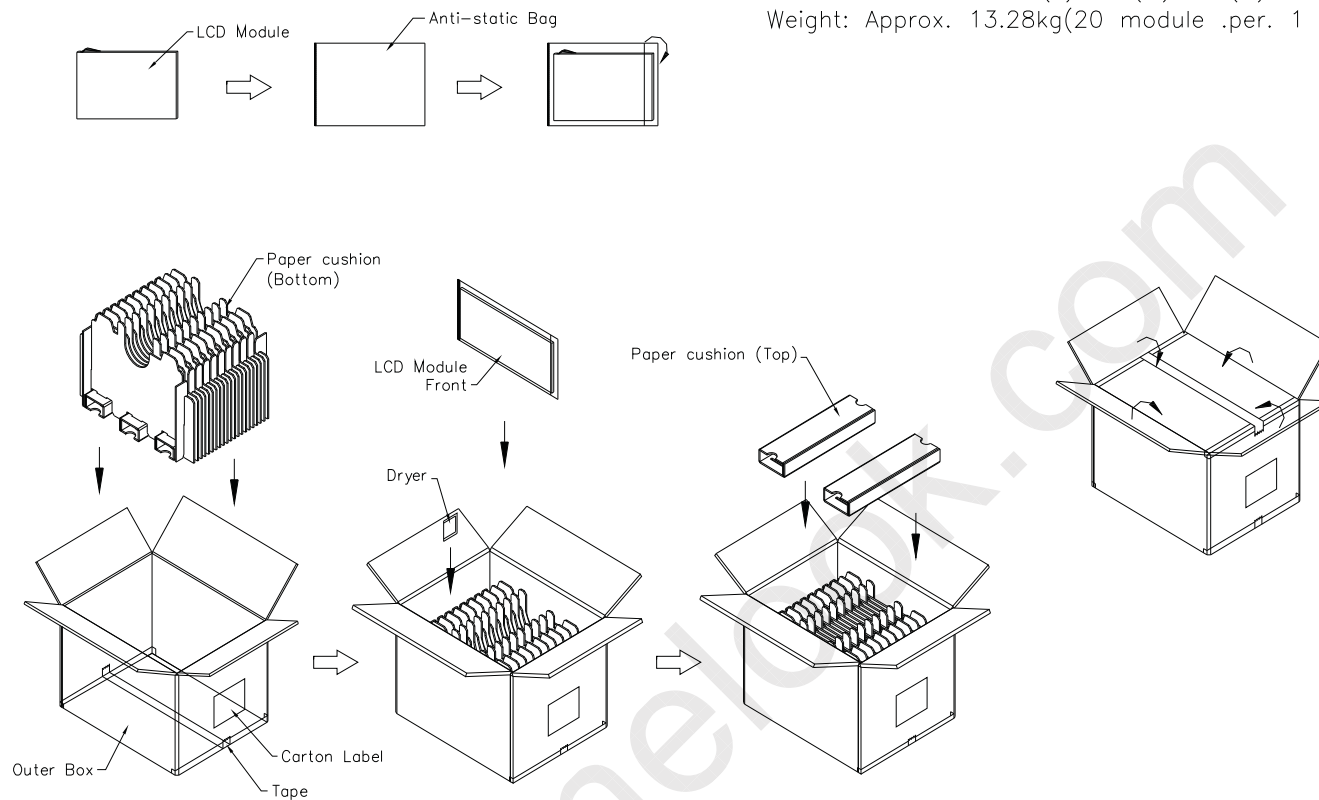
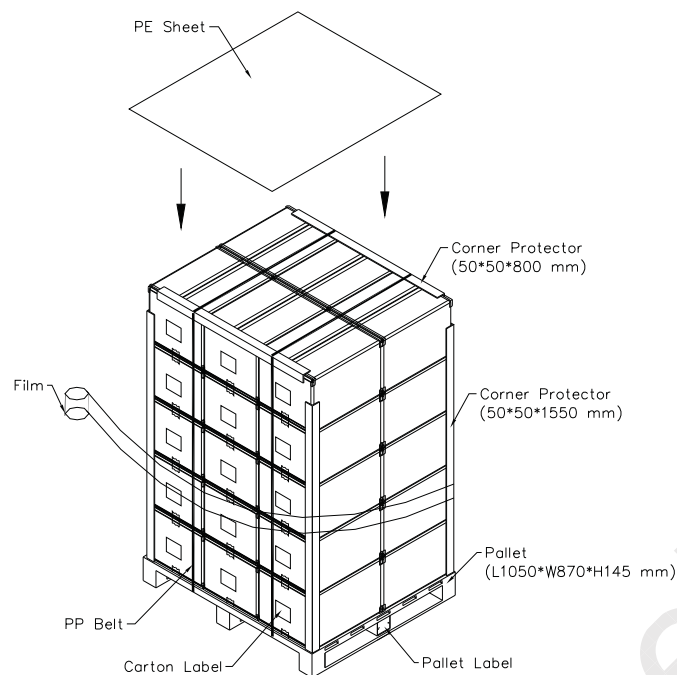


Figure. 9-1 Packing method

9.2 PALLET

Sea & Land Transportation



Air Transportation

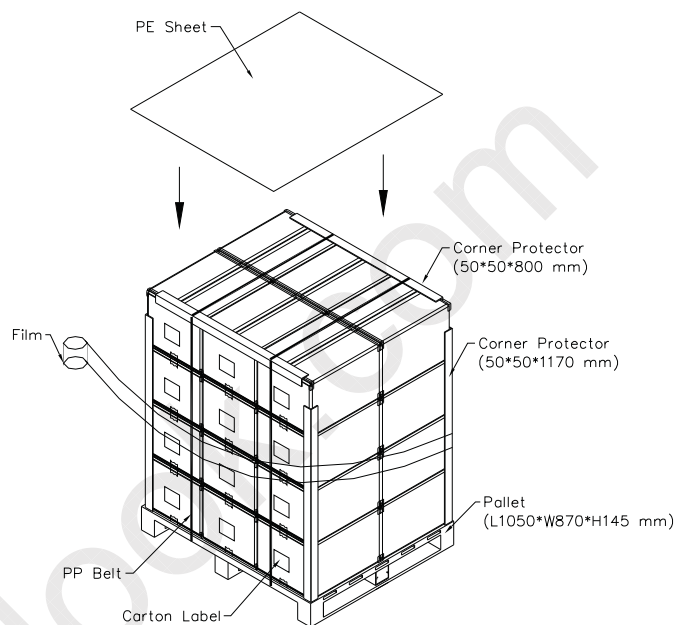


Figure. 9-2 Packing method

10. DEFINITION OF LABELS

CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N154I3 - L02
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: XX XX XX X Y M D X N N N N
 - Serial No.
 - CMO Internal Use
 - Year, Month, Date
 - CMO Internal Use
 - Revision
 - CMO Internal Use
- (d) Production Location: MADE IN XXXX. XXXX stands for production location.
- (e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

Serial ID includes the information as below:

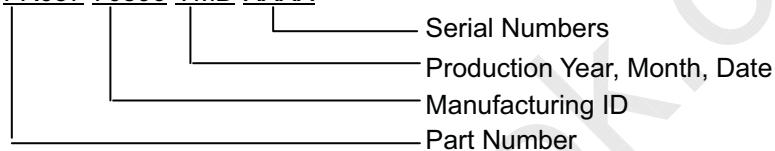
- (a) Manufactured Date: Year: 1~9, for 2001~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

DELL 2D MODULE LABEL

Dell 2D label contains information as below:



(a) Serial ID: TW-0FR037-70896-YMD-XXXX



(b) Production location: Made in XXXX.

(c) Revision code: A00..etc.

CMO CARTON LABEL

CMO carton label is as below:

A rectangular label with a blue header containing the CHI MEI OPTOELECTRONICS logo. Below the header are fields for P.O.NO., Part ID., Model Name, Carton ID., and Quantities. The text "Made in China" is printed at the bottom, along with a GP RoHS logo.

(a) Production location: Made In XXXX. XXXX stands for production location.

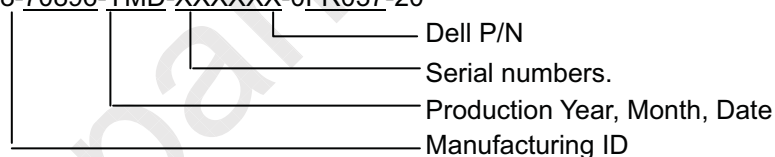
**CHI MEI**
OPTOELECTRONICS CORP.Doc No.:
Issued Date: Nov, 13, 2008
Model No.: N154I3-L02**Approval**

DELL CARTON LABEL

Dell carton label contains information as below:

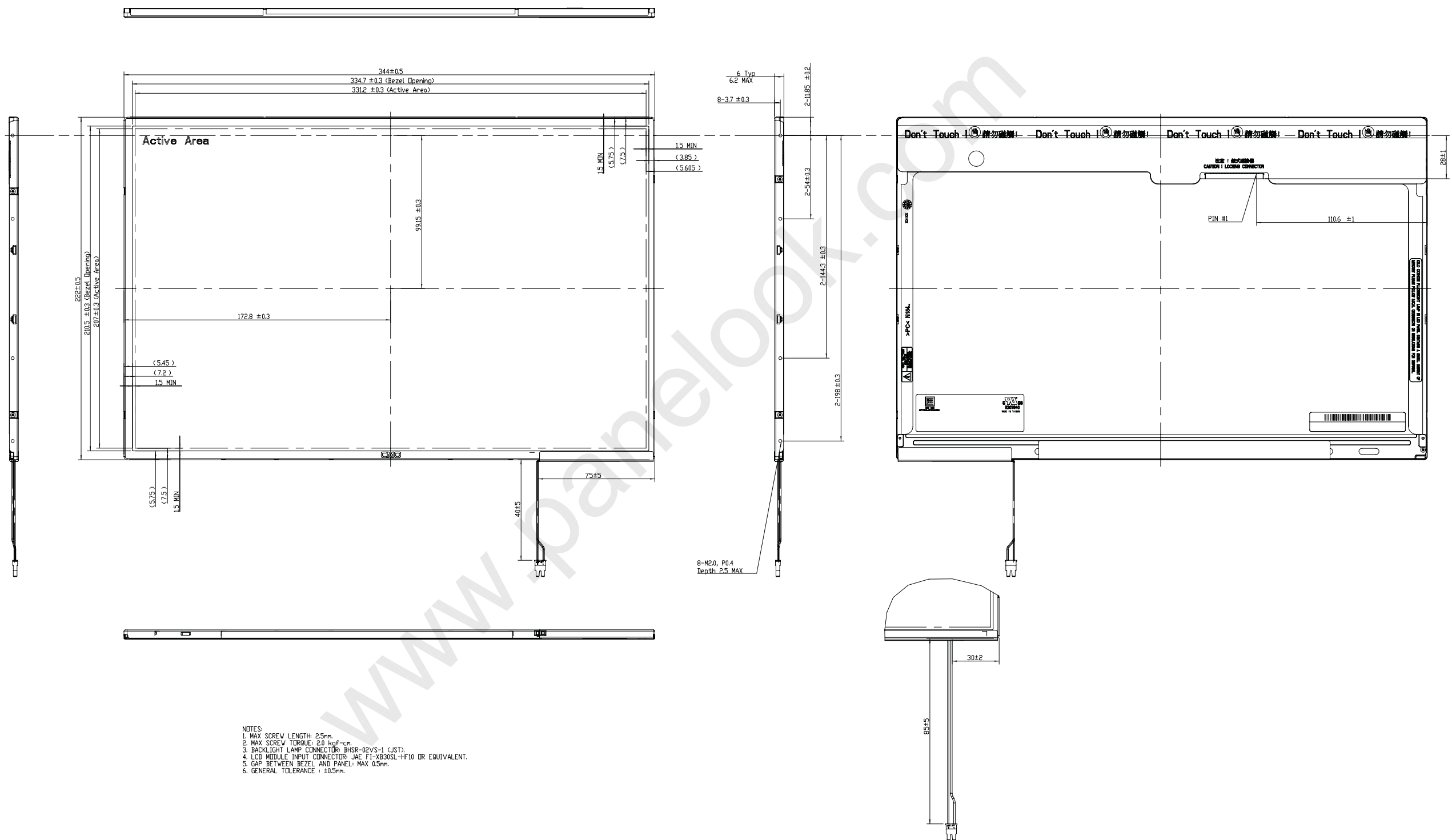


(a) PKG ID: 04688-70896-YMD-XXXXXX-0FR037-20



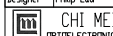
(b) Production location: Made in China

(c) Revision code: A00..etc.



NOTES:
1. MAX. SCREW LENGTH: 2.5mm.
2. MAX. SCREW TORQUE: 2.0 kgf-cm.
3. BACKLIGHT LAMP CONNECTOR: BHSR-02VS-1 (JST).
4. LCD MODULE INPUT CONNECTOR: JAE FI-XB30SL-HF10 OR EQUIVALENT.
5. GAP BETWEEN BEZEL AND PANEL: MAX 0.5mm.
6. GENERAL TOLERANCE: ± 0.5mm.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
1						
2						
3						
4						

TITLE: OUTLINE WITH 6MM WIRE DRAWING NIS413-L02/L03/L04						PD REV. 1A
Approved	Bill Sheu	Drawing No.	NIS40410A			PD REV. 1.6
Checked	Shunnan	Part No.	NA			
Drawn	Jackey Tseng	Material	NA			Sheet 1 / 1 A0
Designer	Philip Lau	Date	7-Mar-2008	Scale	1:1	Unit:mm
 CHI MEI OPTOELECTRONICS CORP.						ALL RIGHTS RESERVED. COPYING FORBIDDEN.